A Pixel Selection Optimization Method for Template Matching Implemented in Small-Scale FPGAs

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***Abstract*— We propose a method for optimizing constraints on pixel selection to reduce the circuit size while suppressing accuracy degradation in the circuit formation of template matching based on pixel selection. It is possible to reduce the number of circuits while maintaining the matching accuracy by selecting a pair of pixels with a smaller co-occurrence probability from left and right pixels at a certain distance from the selected pixel based on the image feature amount.**

I. Background and Purpose

Speeding up template matching is essential from the aspect of industrial application. To handle this issue, several methods have been proposed: the method [1] that calculates the similarity of only pixels selected based on co-occurrence probability. However, these methods do not necessarily consider circuit formation using an ASIC or FPGA.

We propose a template matching method suitable for FPGA circuit construction.

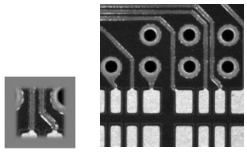
II. Proposed Method and Evaluation Result

We proposed a pixel selection method [2] which selects a pixel selected based on the image feature amount and a right pixel at a fixed distance from the selected pixel as a pair. However, pixels paired with the pixels selected based on the image feature amount in this method are not necessarily effective in matching.

In this research, we propose three selection methods (Constraints 2 to 4) that improve the constraint of always selecting pixels on the right side (Constraint 1) proposed in Reference [2].

Constraint 2 selects a pixel with a lower co-occurrence probability between left and right pixels. The purpose of Constraint 2 is to select a more characteristic one between left and right pixels because the lower co-occurrence probability is, the more characteristic the pixel is.
Constraint 3 selects a pixel with a larger difference in pixel value from the reference pixel between left and right pixels. Constraint 3 expects that a pixel with a larger difference in pixel value from the reference pixel has different characteristics from the reference pixel, and therefore has more information.

In contrast to Constraints 1 to 3, Constraint 4 does not use reference pixels and instead selects pixel pairs in ascending order of their average co-occurrence probability. The purpose of Constraint 4 is to avoid the situation that while the reference pixel is characteristic, a pixel to be paired is not characteristic.



(a) template image (b) input image

Fig.1 Image used for evaluation

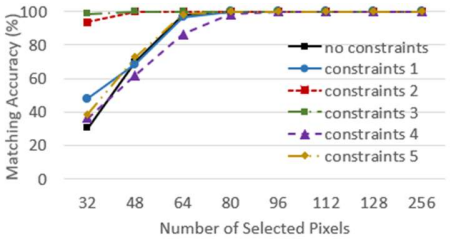


Fig. 2 Evaluation result (matching accuracy)

Constraint 5 is for comparison with Constraint 2. Contrary to Constraint 2, it selects pixels with higher co-occurrence probability among left and right pixels.

Fig. 2 shows the result of evaluating the matching accuracy of Constraints 1 to 5 using the image shown in Fig 1. When the number of selected pixels is 96 or more, the accuracy is almost 100% regardless of the constraints. However, when the number of selected pixels is 80 or less, the matching accuracy of Constraint 2 and 3 is higher than that of other constraints, indicating that the proposed method is effective.

The proposed method can process in 0.7ms on the FPGA evaluation board XCZU7EV (Zynq UltraScale+). The circuit size is 72,891 Slices for LUT, 15,475 Slices for FF, and 2.32 Mb for BRAM.

References

[1] Manabu Hashimoto, Haruhisa Okuda, Kazuhiko Sumi, Takayuki Fujiwara, and Hiroyasu Koshimizu: “High-Speed Image Matching Using Unique Reference Pixels Selected on the Basis of Co-occurrence Probability,” IEEJ Transactions on Industry Applications, 134, 4, (2001) 531

[2] Osamu Nasu, Akiko Yoneta, Yusuke Kawagishi, and Manabu Hashimoto: "A Proposal of a Circuit Size Reduction Method for Template Matching Based on Pixel Selection Using FPGAs,” Symposium on Sensing via Image Information 2023, IS3-02

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